

Defect Luminescence Scanner: Scientific and Industrial-scale Defect Analysis

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In the last decade the interest in silicon carbide (SiC) high-power application devices has significantly grown. Despite great improvements in the material quality of 4H-SiC substrates and epiwafers within the last years, critical defects like stacking faults (SFs) and basal plane dislocations (BPDs) can still lead to bipolar degradation and finally to complete failure of the device. For that reason a new Defect Luminescence Scanner (DLS) based on ultraviolet photoluminescence (UV-PL) imaging [1] has been developed which allows fast, non-destructive and contactless detection of critical defects of 4H-SiC along the device production chain at room temperature [2]. This will not only enable a more efficient optimization of the production process of SiC wafers but will also save time and reduce costs in material and device production, and thereby help to accelerate the further commercialization of SiC power devices.

The DLS system is designed for clean room environment and consists of a 100 mW UV laser operating at 325 nm wavelength for PL excitation, a high-precision sample stage for scanning SiC wafers up to 200 mm, and a PL-optimized microscope setup with a sensitive EMCCD camera for fast image recording with a high signal-to-noise ratio. To get more valuable bulk information we chose a laser excitation of 325 nm. Compared with lower wavelengths, which are more surface sensitive, we obtain a penetration depth of about 7 μm . This allows a detection of surface near defects as well as crystal defects lying in deeper regions of the material, leading to an unprecedented defect detection performance of SFs, BPDs and threading dislocations (TDs) present in substrates, epilayers and partially processed wafers. The standard tool scans the wafer with a field of view of 5 x 5 mm² and a lateral resolution of 5 μm . For example, a full 100 mm wafer can be inspected and characterized in less than five minutes. In addition the camera of the DLS can be optionally equipped with a set of individually selected optical band and long pass filters enabling the identification of different types of SF by their spectral fingerprints [3].

Due to the modular concept of the DLS it is worth mentioning that many features of the system like the spatial resolution, the scan time, all interfaces, the degree of automation, and many other things can be individually adapted to the customer's production or laboratory requirements. In addition the tool will be delivered with an individually tailored software package, including automated defect classification as well as full wafer defect and yield mappings. On request the system can also be delivered with automated wafer handling.

Fig. 1(a) and 1(b) show two typical PL mappings obtained with the DLS from n-type 4H-SiC substrates. The dark spots and lines in Fig. 1(a) correspond to TDs, whereas the dark vertical bar-shaped features close to the wafer edge of Fig 1(b) are identified as SFs. The detailed defect mappings obtained by the DLS do not only allow a better characterization of the substrate quality but also to learn more about the defect generation in epitaxial layers. Figure 1c illustrates a PL image of an n-type epilayer with typical defects like triangular shaped SFs surrounded by a network of BPDs, ingrown particles and pronounced step bunching. After analysing the image data, the corresponding defect and yield mappings can be generated immediately.

Furthermore, the DLS has been used for inline quality control along the device production. Defective electronic devices could be reliably detected and directly sorted out. For example, Fig. 2 shows a PL mapping of a SiC wafer with pn-diodes after p-implantation and high temperature annealing. All pn-diodes containing critical defects, as exemplarily highlighted with red circles for the magnified region, exhibit a significantly increased probability of electrical degradation of the device

performance [4]. This makes the DLS a very powerful tool not only for material characterization but also for inline monitoring along the device production.

Acknowledgment: This work is part of the “SiC-WinS” project funded by the Bavarian Research Foundation (BFS) under contract number AZ-1028-12.

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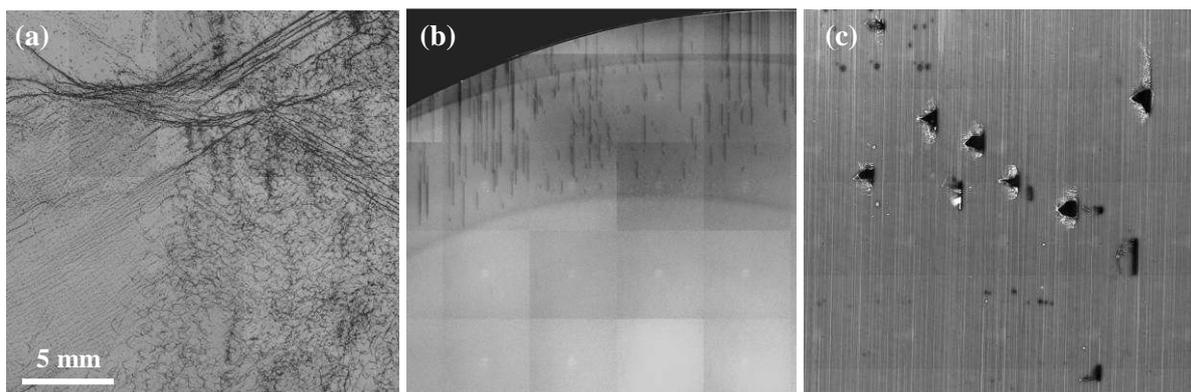


Fig. 1 Examples of typical DLS images of n-type 4H-SiC wafers: PL image of a substrate with a high TD density (a), substrate with a SF cluster at the wafer edge (b), and an epilayer with SFs, BPDs, ingrown particles and pronounced step bunching.

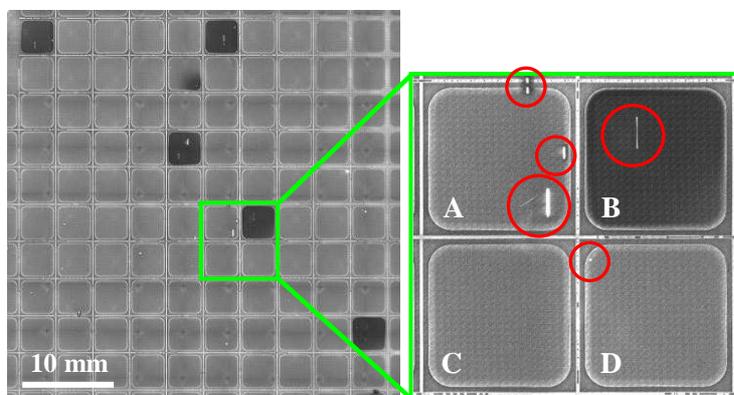


Fig. 2 PL image of a partially processed wafer with 6.5 kV pn-diodes after p-implantation and high temperature annealing. The magnified region shows four diodes of which only device C is defect-free. On the other hand, devices A, B and D show clearly visible defects in the PL imaging and therefore exhibit a significantly increased probability of bipolar degradation.

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